AMENDMENTS TO THE CLAIMS

Claims 1-16 (canceled)

17. (currently amended) A charge pump circuit comprising:

four ~~phase~~ circuits, each of said ~~phase~~ circuits including:

a primary phase circuit; ~~and~~

a respective ancillary phase circuit, said respective ancillary phase circuit[[s]] ~~each~~ serving to control a transistor of said ~~respective~~ primary phase circuit;[[,]] and ~~said four primary phase circuits operated out of phase with one another.~~

a plurality of charge transfer circuits for transferring charge among said four circuits;

wherein said four primary phase circuits are operated out of phase with one another.

18. (previously presented) The charge pump circuit of claim 17, wherein said respective ancillary phase circuits each operate out of phase with one another.

Claims 19-23 (canceled)

24. (currently amended) A charge pump, comprising:

a plurality of single phase charge pump circuits, each comprising a bootstrap capacitor;

a plurality of ancillary charge pump circuits, each respectively associated with one of said plurality of single phase charge pump circuits, and each comprising an ancillary capacitor coupled to the bootstrap capacitor of the associated single phase charge pump circuit; and

a plurality of charge transfer circuits for transferring charge between said plurality of single phase charge pump circuits.

25. (previously presented) The charge pump of claim 24, wherein at least two of said plurality of single phase charge pump circuits are operated in offset phase from another.

26. (previously presented) The charge pump of claim 24, wherein at least two of said plurality of ancillary charge pump circuits are operated in offset phase from another.

27. (currently amended) The charge pump of claim 24, wherein there are four single phase charge pump circuits each operated at an offset phase with respect to the others of said plurality of single phase charge pump[[s.]] circuits.

28. (currently amended) The charge pump of claim 26, wherein said plurality of single phase charge pump circuits comprises:

a first single phase charge pump circuit operating at an initial phase;

a second single phase charge pump circuit operating at a phase angle of 90° relative to said initial phase;

a third single phase charge pump circuit operating at a phase angle of 180° relative to said initial phase; and

a fourth single phase charge pump circuit operating at a phase angle of 270° relative to said initial phase.

29. (currently amended) An integrated circuit, comprising:

a semiconductor substrate;

a charge pump, disposed on said substrate, said charge pump comprising:

a plurality of single phase charge pump circuits, each comprising a bootstrap capacitor and a single phase charge pump output;

a plurality of ancillary charge pump circuits, each respectively associated with one of said plurality of single phase charge pump circuits, and each comprising an ancillary capacitor coupled to the bootstrap capacitor of the associated single phase charge pump circuit;

a plurality of charge transfer circuits for transferring charge among ~~between~~ said plurality of single phase charge pump circuits; and

a charge pump output, coupled to each of said single phase charge pump outputs; and

a first circuit, disposed on said substrate, and coupled to said charge pump output.

30. (previously presented) The integrated circuit of claim 29, wherein at least two of said plurality of single phase charge pump circuits are operated in offset phase from another.

31. (previously presented) The integrated circuit of claim 29, wherein at least two of said plurality of ancillary charge pump circuits are operated in offset phase from another.

32. (currently amended) The integrated circuit [[p]] of claim 29, wherein there are four single phase charge pump circuits each operated at an offset phase with respect to the others of said plurality of charge pumps.

33. (currently amended) The integrated circuit of claim 32, wherein plurality of single phase charge pump circuits comprise:

a first one of said four single phase charge pump circuits operating at an initial phase;

a second one of said four single phase charge pump circuits operating at a phase angle of 90° relative to said initial phase;

a third one of said four single phase charge pump circuits operating at a phase angle of 180° relative to said initial phase; and

a fourth one of said four single phase charge pump circuits operating at a phase angle of 270° relative to said initial phase.

34. (currently amended) An memory device, comprising:

a semiconductor substrate;

a charge pump, disposed on said substrate, said charge pump comprising:

a plurality of single phase charge pump circuits, each comprising a bootstrap capacitor and a single phase charge pump output;

a plurality of ancillary charge pump circuits, each respectively associated with one of said plurality of single phase charge pump circuits, and each comprising an ancillary capacitor coupled to the bootstrap capacitor of the associated single phase charge pump circuit;

a plurality of charge transfer circuits for transferring charge between said plurality of single phase charge pump circuits; and

a charge pump output, coupled to each of said single phase charge pump outputs; and

a memory circuit, disposed on said substrate, and coupled to said charge pump output.

35. (previously presented) The memory device of claim 29, wherein at least two of said plurality of single phase charge pump circuits are operated in offset phase from another.

36. (currently amended) The memory device of claim 29, wherein at least two of said plurality of ancillary charge pump circuits are operated in offset phase from one another.

37. (currently amended) The memory device of claim 29, wherein there are four single phase charge pump circuits each operated at an offset phase with respect the others of said plurality of charge pump[[s.]] circuits.

38. (currently amended) The memory device of claim 32, wherein said plurality of single phase charge pump circuits comprise:

a first single phase charge pump circuit operating at an initial phase;

a second single phase charge pump circuit operating at a phase angle of 90° relative to said initial phase;

a third single phase charge pump circuit operating at a phase angle of 180° relative to said initial phase; and

a fourth single phase charge pump circuit operating at a phase angle of 270° relative to said initial phase.

39. (currently amended) An integrated circuit comprising:

charge pump circuit including,

a first charge pump phase circuit including a first bootstrap capacitor containing stored energy;

a second charge pump phase circuit including a second bootstrap capacitor; and

a circuit, including a flip-flop, for transferring energy from said first bootstrap capacitor to said second bootstrap capacitor to enable said second bootstrap capacitor to utilize energy previously stored in said first bootstrap capacitor to elevate a potential on said second bootstrap capacitor, said transferring occurring in response to a control signal generated by toggling said flip-flop.

40. (currently amended) A memory device comprising:

a memory circuit;

a charge pump circuit, coupled to said memory circuit, said charge pump circuit including:

four ~~phase~~ circuits, each of said ~~phase~~ circuits including:

a primary phase circuit; ~~and~~

a respective ancillary phase circuit, said respective ancillary phase circuit[[s]] ~~each~~ serving to control a transistor of said ~~respective~~ primary phase circuit;[[,]] and ~~said four primary phase circuits operated out of phase with one another.~~

a plurality of charge transfer circuits for transferring charge among said four circuits;

wherein said four primary phase circuits are operated out of phase with one another.

41. (previously presented) The memory device according to claim 40, wherein said respective ancillary phase circuits each operate out of phase with one another.

42. (currently amended) A memory device comprising:

a memory circuit; and

a multi-phase charge pump circuit, coupled to said memory circuit, said multi-phase charge pump circuit comprising:

a plurality of single phase charge pump circuits, including at least:

a first single phase charge pump circuit operating at an initial phase angle;

a second single phase charge pump circuit operating at a phase angle 90 degrees offset from said initial phase angle;

a third single phase charge pump circuit operating at a phase angle 180 degrees offset from said initial phase angle; and

a fourth single phase charge pump circuit operating at a phase angle 270 degrees offset from said initial phase angle; and

~~a plurality of single phase charge pump circuits each including a respective bootstrap capacitor, at least four single phase charge pump circuits of said plurality of signal phase charge pump circuits operated in offset phase from one another; and~~

a charge transfer circuit, adapted to transfer charge between ~~said~~ at least two of said plurality of single phase charge pump circuits. ~~of said plurality of single phase charge pump circuits operated in offset phase from one another, wherein said plurality of single phase charge pump circuits includes at least a first single phase charge pump circuit, a second single phase charge pump circuit, a third single phase charge pump circuit, and a fourth single phase charge pump circuit, each operating at respective phase angles of 0°, 90°, 180°, and 270°.~~

43. (currently amended) A memory device comprising:

a memory circuit; and

a charge pump circuit, coupled to said memory circuit, said charge pump circuit comprising:

a first charge pump phase circuit including a first bootstrap capacitor containing stored energy;

a second charge pump phase circuit including a second bootstrap capacitor; and

a circuit, including a flip-flop, for transferring energy from said first bootstrap capacitor to said second bootstrap capacitor to enable said second bootstrap capacitor to utilize energy previously stored in said first bootstrap capacitor to elevate a potential on said second bootstrap capacitor, said transferring occurring in response to a control signal generated by toggling said flip-flop.